IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Stephen J. Smith et al.
Application No.	:	10/666,948 Confirmation No. 7049
Filed	:	September 19, 2003
For	:	RECONFIGURABLE PROGRAMMABLE LOGIC DEVICE COMPUTER SYSTEM
Group Art Unit	:	2183

New York, New York 10020
January 30, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97, applicants wish to call the attention of the Examiner to the following references:

U.S. Patent Documents

5,068,823	Robinson	11/26/91
5,142,625	Nakai	08/25/92
5,535,342	Taylor	07/09/96
5,548,228	Madurawe	08/20/96
5,684,980	Casselman	11/04/97
5,966,534	Cooke et al.	10/12/99
5,968,161	Southgate	10/19/99
6,085,317	Smith	07/04/00
6,282,627	Wong	08/28/01

Foreign Patent Documents

*1 444 084	Great Britain	07/28/76
EP 0 419 105 A2	EPO	03/27/91
EP 0 445 913 A2	EPO	09/11/91
WO 94/10627	PCT	05/11/94
EP 0 759 662 A2	EPO	02/26/97
WO 97/13209	PCT	04/10/97
EP 0 801 351 A2	EPO	10/15/97
EP 0 829 812 A2	EPO	03/18/98
WO 00/38087	PCT	06/29/00

Other Documents

M. Wazlowski et al., "PRISM-II Compiler and Architecture," IEEE, 1993, pp. 9-16.

David Wo et al., "Compiling to the gate Level for a Reconfigurable Co-Processor," IEEE, 1994, pp. 147-154.

Christian Iseli et al., "A C++ compiler for FPGA custom execution units synthesis," IEEE, 1995, pp. 173-179.

Ian Page, "Constructing Hardware-Software Systems from a Single Description," Journal of VLSI Signal Processing, Vol. 12, No. 1, January 1996, pp. 87-107.

M.D. Edwards, J. Forrest - "Software acceleration using programmable hardware devices," January 1996, pp. 55-63.

Tsuyoshi Isshiki et al., "Bit-Serial Pipeline Synthesis and Layout for Large-Scale Configurable Systems," IEEE, 1997, pp. 441-446.

Luc Séméria et al., "SpC: Synthesis of Pointers in C Application of Pointer Analysis to the Behavioral Synthesis from C," 1998, pp. 340-346.

ELECTRONIK, DE, FRANZIS VERLAG GMBH - "MIT PROGRAMMIERBARER LOGIK VERHEIRATED," March 31, 1998, Vol. 47, No. 7, p. 38.

Michael J. Wirthlin and Brad L. Hutchings - "Improving Functional Density Using Run-Time Circuit Reconfiguration," June 1998, pp. 247-256.

João M.P. Cardoso et al., "Macro-Based Hardware Compilation of Java™ Bytecodes into a Dynamic Reconfigurable Computing System," IEEE, 1999, pp. 2-11.

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"List of FPGA-based Computing Machines," Steve Guccione,<http://www.io.com/~guccione//HW_list.html>, Last modified March 31, 1999.

Timothy J. Callahan et al., "The Garp Architecture and C Compiler," IEEE, April 2000, pp. 62-69.

The aforementioned documents are listed on the accompanying Form PTO-1449 (submitted in duplicate). The document marked with an asterisk (*) is enclosed. All other documents were previously cited by or submitted to the Patent Office in U.S. Patent Application No. 09/443,971, filed November 19, 1999, now U.S. Patent No. 6,658,564 B1, an earlier application from which the above-identified application relies upon for an earlier filing date under 35 U.S.C. § 120. Accordingly, pursuant to 37 C.F.R. § 1.98(d), no copies of these references accompany this Information Disclosure Statement.

It is respectfully requested that the above documents be (1) fully considered by the Patent and Trademark Office during examination of this application; and (2) printed on any patent which may issue on this application. Applicants request that a copy of Form

PTO-1449, as considered and initialed by the Examiner, be returned with the next communication.

Respectfully submitted,

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I hereby certify that this Correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope Addressed to:
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January 30, 2004

Lillian Garcia

Lillian Garcia

Signature of Person Signing

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P.O. Box 1450
Alexandria, Virginia 22313-1450

TRANSMITTAL LETTER FOR
INFORMATION DISCLOSURE STATEMENT

Sir:

Transmitted herewith is an Information Disclosure Statement in the above-identified application. This Statement is submitted:

[ ] within three months of the application filing date;

[X] more than three months from the application filing date but before the mailing date of the first Office Action on the merits.

In accordance with 37 C.F.R. § 1.97, submission of this Statement requires no fee. However, if for any

reason a fee is due, the Director is hereby authorized to charge payment of any fees required in connection with this Information Disclosure Statement to Deposit Account No. 06-1075. A duplicate copy of this letter is transmitted herewith.

Respectfully submitted,

Evelyn C. Mak

Evelyn C. Mak
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Lillian Garcia

Lillian Garcia
Signature of Person Signing

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE
STATEMENT BY APPLICANTS

ATTY. DOCKET NO.	APPLICATION NO.
174/161 Cont.	10/666,948
APPLICANTS	**CONFIRMATION NO.**
Stephen J. Smith et al.	7049
FILING DATE	**GROUP ART UNIT**
September 19, 2003	2183

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5,068,823	11/26/91	Robinson	395	500	
	5,142,625	08/25/92	Nakai	395	275	
	5,548,228	08/20/96	Madurawe	326	41	
	5,535,342	07/09/96	Taylor	395	307	
	5,684,980	11/04/97	Casselman	395	500	
	5,966,534	10/12/99	Cooke et al.	395	705	
	5,968,161	10/19/99	Southgate	712	37	
	6,085,317	07/04/00	Smith	713	1	
	6,282,627	08/28/01	Wong	712	15	

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						YES	NO
	1 444 084	07/28/76	Great Britain	H03K	19/00		
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	EP 0 445 913 A2	09/11/91	EPO	G06F	15/60		
	WO 94/10627	05/11/94	PCT	G06F	5/00		
	EP 0 759 662 A2	02/26/97	EPO	H03K	19/177		
	WO 97/13209	04/10/97	PCT	G06F	17/50		
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EXAMINER **DATE CONSIDERED**

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANTS	ATTY. DOCKET NO. 174/161 Cont.	APPLICATION NO. 10/666,948
	APPLICANTS Stephen J. Smith et al.	CONFIRMATION NO. 7049
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